

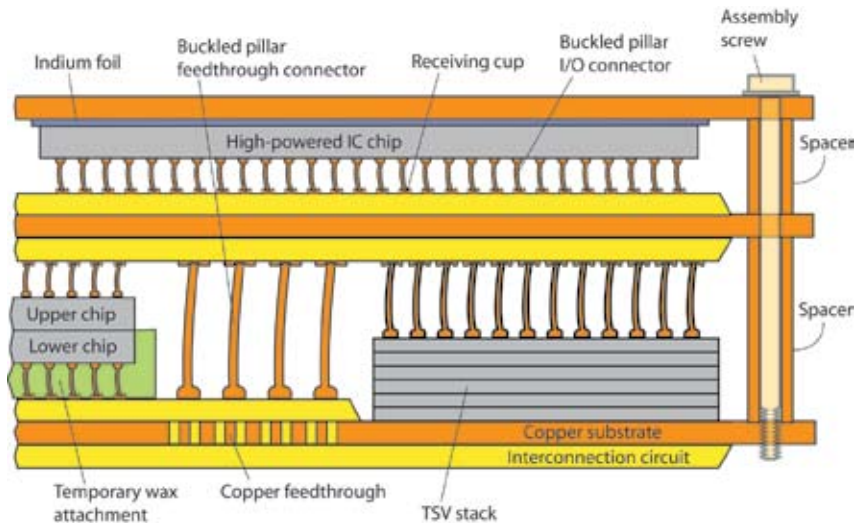
# Solder-Free Connectors Using Buckled Pillars

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**A** particularly versatile form of wafer bumping is stud bumping<sup>(1)</sup>, using either gold or copper wire. The equipment required is an adaptation of a traditional wire bonder. A ball bond is made at a first contact pad using heat and ultrasonic energy. The wire is extended in a precise direction and a flying lead is created by terminating the wire, for example using electronic flame-off (EFO). This type of stud bump can be used as a buckled pillar connector, enabling electronic assemblies that are put together with screws rather than solder. With appropriate assembly and testing techniques, this can lead to waste-free integrated assemblies; no good parts are thrown away due to compound yield problems, otherwise known as “known good die” or KGD problems.

## Why Replace Ball Grid Array (BGA) Packaged Devices?

BGA has become the dominant packaging type for electronic systems, representing 60% of the total packaging revenue in 2008<sup>(2)</sup>. More and more BGA packages employ a method of direct chip attach (DCA) called “flip chip”<sup>(3)</sup>. IBM created the first BGA packages in 1965, using the C4 process. Recently it has created the C4NP process<sup>(4)</sup>, “Controlled Collapse Chip Connection New Process”. C4NP was developed to improve yield and reliability while reducing cost. However, BGA and C4NP still have two serious drawbacks. First, an epoxy underfill is normally required for die sizes larger than around 4mm. The underfill binds the chip and the substrate together to make a robust package that can withstand the differential stresses induced by temperature cycling, as well as withstand increased levels of shock and vibration. This is a big factor in helping your cell phone survive being dropped. However, the epoxy can not be easily removed if a chip fails in an integrated assembly. The failure could be a subtle flaw that was not detected by the component test program, or it could be assembly-induced. Since the underfill step can not be undone, rework is limited or impossible. For an integrated electronic assembly, rework is the process of finding a defective chip and replacing it. Not having



**Figure 1. Customized buckled pillar connectors support many assembly configurations.**

a viable path for rework presents a serious economic disadvantage. It means for example that stacked die assemblies employing underfill will incur an additional cost due to compound yield issues. It also means that integrated assemblies employing underfill are limited to around 5 or 6 die, because reject costs become too great for more complex assemblies. Finally the underfill itself adds both material and process cost.

The second big disadvantage with BGA and C4NP is that they both employ solder. The solder may be lead-free, but it still contributes to environmental and reliability problems<sup>(5)</sup>. Solder is reputed to cause more failures in electronic assemblies than any other single cause; the failures range from solder bridging (shorts), to open traces, to corrosion, creep, cracking at brittle intermetallic interfaces, and tin whiskers.

## The Buckled Pillar Solution

Figure 1 is a conceptual drawing showing the versatility of buckled pillar connectors in a new type of integrated assembly. The buckled pillars are formed by a manufacturing sequence that is described in detail in reference 6, including an animation of the process steps.

In Figure 1, buckled pillars having potentially five different lengths are required. Because the bonding tool follows a programmed sequence, the different lengths are easily accommodated in an automated fashion. Components are aligned and placed, and the entire assembly is compressed using assembly screws provided in each corner. The screws work against spacers to provide exactly the right amount of compression,

enough to buckle the pillars by a few percent in length. This means that the bonding wire material is not stressed above its elastic limit; accordingly it acts like a spring. This helps to provide good electrical contact at the receiving cup end, and also provides some design margin to accommodate minor differences in co-planarity of the tips of the buckled pillars.

The system assembly can accommodate stacked components that employ through silicon vias (TSVs), but TSVs are not required in all of the chips. The TSV stacked component in the figure represents a complex component having very high electrical performance, but at a considerable cost. The additional cost is associated with the intricate processing to form the through vias. This will typically represent a good economic alternative only for the highest production volumes. The module or system-level assembly method depicted in the figure accommodates many heterogeneous chip types. Nearly all chips that are currently in use via other assembly techniques (such as conventionally packaged devices on printed circuit boards (PCBs), can be used in the compact assembly of Figure 1. The conventional packages are eliminated, providing a substantial cost benefit as well as contributing to a more standard electrical, thermal, and mechanical environment. Packages of today encompass so many different types and incorporate so many different design rules with respect to signal integrity and thermal issues as examples; they have become a burden with respect to the design goal of a standardized environment.

It may also be desirable to create semiconductor chip versions of discrete components such as resistors and bypass capacitors, integrating many of these on each chip. The pad pitch can be as fine as 50  $\mu\text{m}$ , using 20  $\mu\text{m}$  wire<sup>(7,8)</sup>. Since the ball bond is formed robustly using heat and ultrasonic energy, nearly all pad metals and underbump metallurgies can be accommodated.

Note that none of the connections include solder. This leads to convenient rework scenarios, wherein a module can be disassembled and a defective chip replaced, using only a placement machine having good alignment capabilities and a screw-driver.

High power IC chips may be provided in a single-high layer at the top of the module as shown. Preferably a soft conductive material such as indium foil will be provided at the silicon-copper interface, for the best possible thermal connection. If electrical isolation is required at the back side contact of the chip, a thin coating of silicon nitride can be used. The indium foil fills microscopic voids and helps to eliminate air pockets at the interface. The exposed copper surface at the top of the module is available for heat sinking, providing very low thermal impedance between the transistor junctions in the chip and the heat sink material.

In Figure 1 the substrates are preferably made of copper, and fabricated in a large panel size such as 12 x 18 inches. The use of copper provides good heat distribution and enables the use of a water coolant between module layers. Since the power density in such an assembly is much higher than in a regular PCB assembly, good heat distribution and extraction become mandatory. The interconnection layers shown in yellow are preferably fabricated using direct laser imaging, and this combination of copper cores and laser imaging has recently become available. The build-up layers of the interconnection circuits can be fabricated using fine geometries such as 30  $\mu\text{m}$  line and space<sup>(9)</sup>, again supporting the miniaturized assembly.

### Options for External Connections

In Figure 2(a), solder balls have been formed at the bottom face of the module, and the system in package (SIP) presents a BGA interface to the outside world. In Figure 2(b), buckled pillar connections are shown for interfacing between the SIP and a conventional PCB. Figure 2(c) shows that a flex circuit equipped with buckled pillar connectors may be used for external signals.

### A New Cost Tradeoff

Good cost figures are not yet available for miniaturized 3D assemblies as shown in Figure 1. The build-up technology on copper is substantially more expensive than regular PCB technology employing epoxy-glass laminates. However, a system-level cost

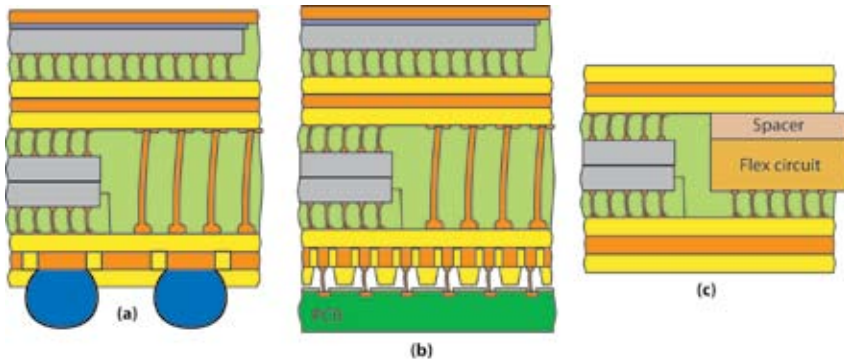


Figure 2. BGA, buckled pillar, and flex circuit options for external connections.

analysis will take into account the following factors: (i) conventional packages for each IC chip are eliminated; (ii) the availability of effective rework strategies may lower the cost of yielded assemblies; (iii) the resulting assembly will be more compact and more power efficient leading to savings in space and energy consumption. To illustrate this last point, energy consumption in data centers is currently estimated at 20% of operating costs, and power equipment plus cooling equipment add an additional 24%<sup>(10)</sup>. In addition, once the technology has been shaken down, superior reliability may result from eliminating solder, leading to reduced cost from failures in the field.

### Where Will This Technology Be Used?

3D assemblies enabled by buckled pillar connectors are a natural fit with high-powered systems such as servers and routers. For blade servers, it is estimated that the new 3D assemblies can reduce space requirements by as much as 50X and weight requirements by as much as 20X. Accordingly, they may become an attractive option for aerospace applications.

### Remaining Challenges

Although stud bumping machines exist with the necessary adaptations for making buckled pillar connectors, they are not yet produced by mainstream suppliers and are not yet commercially available. Although lapping and chemical mechanical polishing (CMP) machines and processes exist for planarizing the tips of the pillars, specific processes are still under development. Mechanical modeling is required to confirm the elastic behavior of copper and gold pillars, for specific implementations of wire diameter, pillar length, and compression factor. In the absence of a supporting medium such as wax, the buckled pillars must adequately support the embedded chips. Although good shock performance may be achievable with the flexible pillars, this must be confirmed by modeling and experiment. If the technology is combined with water cooling, the primary issue relates to water seals between copper elements. Hydrophobic wax may be used to keep water away from electronic components, but this must be tested and limits the maximum operat-

ing temperature to around 90°C. To take advantage of the proposed more-standardized design environment (excluding chip packages), new design software must be developed and existing software must be integrated into convenient tools. However, the new software may enjoy a much larger market due to wide applicability of the standardized environment.

### Conclusion

Although much work remains to validate and test the proposed 3D structures, the potential benefits are substantial. Building on the versatility of stud bumping machines, the overall technique is versatile and can be adapted to many different substrates and chip stack configurations. Compaction factors as high as 50X may be achievable while providing adequate heat removal, effective re-workability, and high reliability. Almost all IC chips that are in use today can be utilized without modification. Although no through silicon vias (TSVs) are required, TSV stacks can be accommodated. Using copper substrates, water cooling may become a practical option. ◆

Credit: This article will appear in the January/February 2009 issue of *Advanced Packaging Magazine*.

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